AMENDMENTS TO THE SPECIFICATION

Please amend the following paragraph.

On page 4, paragraph [0010]:

In some aspects, the invention relates to an apparatus for reducing signed load latency in a microprocessor. The apparatus includes: a data path connecting a ~~cash~~ cache memory to an aligner; and a bypass connecting the ~~cash~~ cache memory to the aligner. The data is transferred from the cache memory to the aligner via the data path, and a sign bit for the data is transferred ~~to~~ from the cache memory to the aligner via the bypass. In some embodiments, the apparatus further includes a select component for providing a signal to generate the sign bit for the data. In some embodiments, the bypass includes a sign multiplexer and a real-sign multiplexer.